REMARKS

In the Drawings

The disclosure was objected to because the specification mentions "a synchronous bus 202", on page 4, in reference to figure 2; however, number 202 did not appear in the figure. Figure 2 has been amended to include the reference number 202 in the appropriate location as described in the specification. No new matter has been entered by this amendment.

Double Patenting Rejection

Claims 1-20 were provisionally rejected under the judicially created obviousness-type double patenting as being unpatentable over claims 1-21 of copending U.S. Patent Application Serial No. 09/943,476 in view of *Dye* (U.S. Patent No. 6,145,069). The figures and specification of *Dye* show a compression engine 260 and a decompression engine 280 in a flash memory system. This reference teaches away from Applicant's present invention in which a flash memory device receives the compressed data from a processor and the flash memory only has the capability of decompressing the data as it is being transferred. Therefore, even if it were obvious to combine *Dye* with co-pending SN 09/943,476, and Applicant maintains that it is not, the combination cannot render the present application unpatentable.

Claim Rejections Under 35 U.S.C. §112

Claim 18 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that there is insufficient antecedent basis for the limitation in the claim "the synchronous memory device" in line 1. Claim 18 has been amended to overcome the rejection under 35 U.S.C. §112, second paragraph.

Claims 19 and 20 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner stated that the limitations "the synchronous memory" and "the non-volatile memory" lacked antecedent basis. Claims 19 and 20 have been amended to overcome the rejection under 35 U.S.C. §112, second paragraph.

Claim Rejections Under 35 U.S.C. §102

Claims 1, 3-5, 11, 14 and 15 were rejected under 35 U.S.C. §102(e) as being anticipated by *Dye* (U.S. Patent No. 6,145,069). Applicant respectfully traverses this rejection.

Dye teaches a flash memory controller that uses data compression/decompression for improved system performance. The figures and specification of Dye show a compression engine 260 and a decompression engine 280. This reference not only does not disclose the Applicant's invention as claimed in the amended claims, it actually teaches away from Applicant's invention.

Applicant's claimed invention does not contain a compression engine. As clearly explained in the present specification (see page 4, paragraph 0015) and claimed in the claims, the compressed data of the present invention is provided only by the system processor. The memory device, therefore, contains only the decompression algorithm.

Claims 11, 12 and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by *Fallon et al.* (U.S. Patent Publication No. 2002/0069354). Claims 1, 4 and 14 were rejected under 35 U.S.C. §102(e) as being anticipated by *Iverson* (U. S. Patent No. 6,332,172). Applicant respectfully traverses this rejection.

Claims 11 – 15 have been cancelled without prejudice. Claim 18 has been amended to depend from independent claim 16 that subsequently is shown to be patentable over the art of record.

Iverson discloses a method for virtual memory compression in which a compressed image is stored in flash memory. *Iverson* neither teaches nor suggests Applicant's invention of a non-volatile memory comprising the capability of decompressing stored compressed data as it is being transferred out to volatile memory. Figures 6 and 7 of *Iverson* clearly show that the decompression is performed by a separate block such as the decompressor 612 of Figure 6 or the decompressor 712 portion of the CPU 702 of Figure 7.

Claim Rejections Under 35 U.S.C. §103

Claims 1, 2, 5-7 and 9 were rejected under 35 U.S.C.§ 103(a) as being unpatentable over *Harari et al.* (U.S. Patent No. 6,266,724) in view of *Fallon*. Applicant respectfully traverses this rejection.

Harari et al. discloses a mother card 10 that includes a controller 41 and functional modules 42. Two of the possible functions of these modules 42 are the compression and

decompression of data. A daughter card 20 can carry memory for the system. *Harari et al.* neither teaches nor suggests Applicant's invention of the processor providing the compressed data and the non-volatile memory device having the decompression circuit. The compressed data of *Harari et al.* is provided by the same functional module 42 and not the controller 41.

Harari et al. also teaches that the functional module 42 that performs both the compression and decompression is separate from the daughter card (20) that contains the memory. Applicant's present invention is to a decompression circuit that is included in the flash memory device. This is neither taught nor suggested by *Harari et al.*

Since *Fallon* discloses only a DRAM it cannot teach or suggest Applicant's invention. Since neither *Harari et al.* nor *Fallon* teach or suggest Applicant's invention as claimed, the combination of these references cannot teach or suggest Applicant's invention.

Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Baltz et al.* (U.S. Patent No. 6,058,474) in view of *Harari*. Applicant respectfully traverses this rejection. As discussed previously, independent claim 6, from which claim 8 depends, has been shown to be patentable over the art of record. Therefore, claim 8 is patentable for the same reasons.

Claims 16, 17 and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Baltz et al.* in view of *Iverson*. Applicant respectfully traverses this rejection.

Baltz et al. discloses a method for DMA boot loading a microprocessor. When a reset signal is de-asserted, a boot load operation is performed. *Iverson* discloses a method for virtual memory compression in which a compressed image is stored in flash memory. Neither *Baltz et al.* nor *Iverson* teach or suggest a flash memory device that comprises a decompression capability that decompresses and transfers data to a synchronous memory after a reset signal and then provides a system reset signal to a processor after transfer of the data. Since neither reference individually teaches or suggests Applicant's invention as claimed, even if it were obvious to combine *Baltz et al.* with *Iverson*, the combination would not teach or suggest Applicant's invention.

Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Fallon* in view of *Shin* (U. S. Patent No. 6,735,669). Claim 13 has been cancelled without prejudice.

Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Harari* in view of *Fallon*. Claim 10 depends from independent claim 6 that has previously been shown to be patentable over the art of record. Therefore, claim 10 is also patentable over the art of record.

Claim 20 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Baltz et al.* in view of *Iverson* as applied to claim 19 above further in view of *Shin*. Applicant respectfully traverses this rejection.

Claim 20 is not obvious over *Baltz et al.* in view of *Iverson* and *Shin* for the above-stated reasons with respect to the rejection of claims 16, 17, and 19. *Shin* simply adds a RAMBUS DRAM but does not teach or suggest a flash memory device that has decompression capability as claimed in the present application. Therefore, even if it were obvious to combine *Baltz et al.*, *Iverson*, and *Shin*, claim 20 would not be obvious over the combination.

CONCLUSION

For the above reasons, Applicant requests that the Examiner withdraw the rejections and allow the present claims. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

Date: 18August2004

Daniel J. Polglaze
Reg. No. 39,801

Attorneys for Applicant
Leffert Jay & Polglaze
P.O. Box 581009
Minneapolis, MN 55458-1009
T 612 312-2200
F 612 312-2250